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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371				U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 10/049388	
INTERNATIONAL APPLICATION NO. PCT/SG99/00084		INTERNATIONAL FILING DATE 13 August 1999		PRIORITY DATE CLAIMED	
TITLE OF INVENTION <p style="text-align: center;">A SWITCH CIRCUIT</p>					
APPLICANT(S) FOR DO/EO/US <p style="text-align: center;">Jun MAKINO</p>					
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:					
<ol style="list-style-type: none"> 1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371. 2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371. 3. <input type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below. 4. <input checked="" type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31). 5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2)) <ol style="list-style-type: none"> a. <input type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau). b. <input checked="" type="checkbox"/> has been communicated by the International Bureau. c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US). 6. <input type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)). <ol style="list-style-type: none"> a. <input type="checkbox"/> is attached hereto. b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4). 7. <input type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)) <ol style="list-style-type: none"> a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau). b. <input type="checkbox"/> have been communicated by the International Bureau. c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired. d. <input type="checkbox"/> have not been made and will not be made. 8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)). 9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). - unsigned 10. <input type="checkbox"/> An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)). 					
Items 11 to 20 below concern document(s) or information included:					
<ol style="list-style-type: none"> 11. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98. 12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. 13. <input checked="" type="checkbox"/> A FIRST preliminary amendment. 14. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment. 15. <input type="checkbox"/> A substitute specification. 16. <input type="checkbox"/> A change of power of attorney and/or address letter. 17. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with 37 CFR 1.81. 18. <input type="checkbox"/> A second copy of the published international application and English language translation. 19. <input type="checkbox"/> A second copy of the English language translation of the international application. 20. <input checked="" type="checkbox"/> Other items or information: 7 sheets of drawings. 4 references. PEFS print form. Postcard 					

EXPRESS MAIL CERTIFICATE

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Dorothy Jenkins

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Dorothy Jenkins

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February 12, 2002

Date of Signature

P/2778-25

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Jun MAKINO

Date: February 12, 2002

Serial No.:

Group Art Unit:

Filed:

Examiner:

For: A SWITCH CIRCUIT

U.S. Patent and Trademark Office

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AMENDMENT/SUBMISSION

Prior to examination, please amend the application as follows.

FEE CALCULATION

Any additional fee required has been calculated as follows:

_____ If checked, "Small Entity" status is claimed.

	NO. CLAIMS AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR		EXTRA PRESENT		RATE		ADDIT. FEE
TOTAL	14	MINUS	20	* =	0	X	(\$9 SE or \$18)		\$
INDEP.	1	MINUS	3	** =	0	X	(\$42 SE or \$84)		\$
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM						X	(\$140 SE or \$280)		\$
* not less than 20 ** not less than 3									TOTAL \$ -----

If any additional payment is required, a check which includes the calculated fee of \$ _____
 (OFGS Check No. _____) is attached.

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

CONTINGENT EXTENSION REQUEST

If this communication is filed after the shortened statutory time period had elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. § 1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. § 1.135. The fee under 37 C.F.R. § 1.17 should be charged to our Deposit Account No. 15-0700.

AMENDMENTS

☒ If checked, amendment(s) to the specification and/or claims are submitted herewith.

1. ☐ If checked, an abstract is submitted as the last page of Appendix A.

2. Claims:

Please cancel claims _____ without prejudice.

Please amend claims 6, 7, 9-11, 13 and 14 pursuant to 37 C.F.R. § 1.121(c)(i) as set forth in the "clean" version attached hereto as Appendix A. Entry is respectfully requested. A version with markings to show the changes made pursuant to 37 C.F.R. § 1.121(c)(ii) is attached hereto as Appendix B.

☐ If checked, the optional complete set of "clean" claims pursuant to 37 C.F.R. § 1.121(c)(3) is attached hereto as Appendix C.

REMARKS/ARGUMENT

This Preliminary Amendment is being submitted to change the multiple dependent claims to single dependent claims in order to eliminate the improper multiple dependent claims and to reduce the government filing fee.

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Dorothy Jenkins
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February 12, 2002

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APPENDIX A
“CLEAN” VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

CLAIMS (with indication of amended or new):

(Amended) 6. A switch circuit according to claim 1, wherein the first transistor is a bipolar transistor.

(Amended) 7. A switch circuit according to claim 1, wherein the first transistor is a MOSFET.

(Amended) 9. A switch circuit according to claim 6, wherein the second and third transistors are bipolar transistors.

(Amended) 10. A switch circuit according to claim 7, wherein the second and third transistors are MOSFETs.

(Amended) 11. A switch circuit according to claim 1, wherein the pulse generation device comprises a capacitance device.

(Amended) 13. A switch circuit according to claim 1, further comprising a first signal input contact coupled to the activating input of the electronic switching device.

(Amended) 14. A switch circuit according to claim 3, further comprising a second signal input contact coupled to the collector of the third transistor and the base of the second transistor.

APPENDIX B
VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

CLAIMS:

6. A switch circuit according to [any of the preceding claims] claim 1, wherein the first transistor is a bipolar transistor.

7. A switch circuit according to [any of claims 1 to 5] claim 1, wherein the first transistor is a MOSFET.

9. A switch circuit according to claim 6 [when dependent on any of claims 3 to 5], wherein the second and third transistors are bipolar transistors.

10. A switch circuit according to claim 7 [or claim 8 when dependent on any of claims 3 to 5], wherein the second and third transistors are MOSFETs.

11. A switch circuit according to [any of the preceding claims] claim 1, wherein the pulse generation device comprises a capacitance device.

13. A switch circuit according to [any of the preceding claims] claim 1, further comprising a first signal input contact coupled to the activating input of the electronic switching device.

14. A switch circuit according to [any of claims 3 to 5, or any of claims 6 to 13 when dependent on any of claims 3 to 5] claim 3, further comprising a second signal input contact coupled to the collector of the third transistor and the base of the second transistor.

A SWITCH CIRCUIT

The invention relates to a switch circuit and in particular, a switch circuit including a momentary switch.

Momentary switches for turning on and off electrical and electronic equipment operate using a logic type operation so that when a switch pulse is supplied to a switch circuit, the circuit switches from "off" to "on" or from "on" to "off". The switch pulse is provided by actuation of the momentary switch which when actuated completes the circuit to provide a pulse to the switch circuit to switch the state of the switch circuit.

It is common practice for a number of different types of electrical and electronic equipment to use only a single momentary switch to switch the equipment both on and off.

However, one of the disadvantages of using a single momentary switch is that, during the off state, it is still necessary for power to be supplied to the switch circuit. This is because it is necessary to maintain a live switch circuit for sensing a switch pulse generated by the momentary switch at any time. Therefore, this power consumption constantly drains the battery or AC power even though the electronic equipment appears to be in an "off" state to a user.

This consumption of electrical power is especially important to battery operated equipment such as laptop computers and

mobile (or hand) phones where the constant power requirement drains the battery even when the equipment is switched off.

For example, in a typical laptop computer, the power consumption when the computer is switched off can be as high as 8 mA, which would mean that a 3300 mAh battery would be completely drained after seventeen days even with the laptop computer switched off. Where the computer has a smaller battery, the duration will be even less. For example, if the battery is only a 1800 mAh battery, the battery will be drained in only nine days even with the computer switched off all the time.

A similar problem exists with other equipment using momentary switches such as mobile phones, where the power consumption while the phone is switched off still leads to draining of the battery.

In accordance with the present invention, there is provided a switch circuit for controlling the supply of electrical power from an electrical power source to a load, the switch circuit comprising a first transistor, the emitter of the first transistor adapted to be coupled to the power supply and the collector adapted to be coupled to the load; an electronic switching device comprising an input, an output adapted to be coupled to the other side of the load and the power source, and an activating input; a first resistance device coupled between the base of the first transistor and the input of the

electronic switching device; a momentary switch having first and second terminals, the activating input of the electronic switching device coupled to the first terminal of a momentary switch; a pulse generation device coupled between the collector of the first transistor and the second terminal of the momentary switch; and a charge storing device coupled between the collector of the first transistor and the output of the electronic switching device.

Preferably, the first transistor is a bipolar transistor, and more preferably a pnp bipolar transistor.

However, alternatively, the first transistor may be a MOSFET, such as an enhancement type MOSFET, and is typically a P channel enhancement type MOSFET.

Typically, the electronic switching device comprises a thyristor device, such as a transistor device and preferably comprises second and third transistors. The second and third transistors are typically bipolar transistors, one transistor being an npn transistor and the other being a pnp transistor. Preferably, where the first transistor is a pnp bipolar transistor, the second and third transistors are npn and pnp bipolar transistors, respectively.

However, where the first transistor is a P channel enhancement type MOSFET, the second and third transistors are N and P channel enhancement type MOSFETs, respectively.

Preferably, the base of the second transistor is coupled to the collector of the third transistor, and the base of the third transistor is coupled to collector of the second transistor.

Typically, the input to the electronic switching device is coupled to the emitter of the third transistor, the output is coupled to the emitter of the second transistor, and the activating input is coupled to the base of the third transistor and the collector of the second transistor.

Typically, the switch circuit may also comprise a first signal input contact coupled to the activating input of the electronic switching device which permits the switch circuit to be switched on using an electrical signal. Typically, the switch circuit may be switched on by applying a voltage with a sufficiently low magnitude to the signal input contact to forward bias the base of the third transistor.

Alternatively, the first signal input contact may be used to switch the switch circuit off by applying a voltage of a sufficiently high magnitude to reverse bias the base of the third transistor.

Typically, the switch circuit may further comprise a second signal input contact coupled to the collector of the third transistor and the base of the second transistor, to permit the electronic switching device to be switched off, and

therefore, the first transistor to be switched off, by applying an electrical signal to the second signal input contact. Typically, the electrical signal applied to the second signal input contact is a ground signal.

The advantage of the first and second signal input contacts are that they permit the switch circuit to be switched off by the electronic equipment being supplied by the power supply without requiring activation of the momentary switch. Alternatively, the first and second signal input contacts permit the switch circuit to be switched on and off by a remote system, without requiring activation of the momentary switch.

Preferably, the pulse generation device comprises a capacitance device and typically, a third resistance device in parallel with the capacitance device.

Typically, the switch circuit further comprises a fourth resistance device coupled between the emitter and base of the first transistor and a fifth resistance device coupled between the base of the second transistor and the output of the electronic switching device.

Examples of a switch circuit in accordance with the invention will be now be described with reference to the accompanying drawings, in which:-

Figure 1 is a circuit diagram of a first example of a switch circuit with a momentary switch in an open position;

Figure 2 is a circuit diagram of the switch circuit of Figure 1 with the momentary switch in a closed position during switching on of the switch circuit;

Figure 3 is a circuit diagram of the switch circuit of Figure 1 with the momentary switch in a closed position during switching off of the switch circuit;

Figure 4 is a circuit diagram of a second example of a switch circuit;

Figure 5 is a circuit diagram of a third example of a switch circuit;

Figure 6 is a circuit diagram of a fourth example of a switch circuit;

Figure 7 is a schematic diagram showing the switch circuit of Figures 1 to 3 being used to control electrical power from a rectified AC mains supply;

Figure 8 is a schematic diagram showing the switch circuit of Figures 1 to 3 being used to control an AC power supply for a high power consumption load; and,

Figure 9 is a circuit diagram of a fifth example of a switch circuit.

Figure 1 is a circuit diagram showing a switch circuit 10 which acts as an interface between a power supply in the form of a battery 11 and a load represented by resistor R5. The switch circuit 10 includes a pnp bipolar transistor Q1 with

the emitter of the transistor Q1 coupled to the positive terminal of the battery 11. The collector terminal of the transistor Q1 is connected to one side of the load R5. A resistor R8 is coupled between the emitter terminal and the base terminal of the transistor Q1. The base of the transistor Q1 is also coupled to the emitter of a second transistor Q3 via a resistor R1. The transistor Q3 is also a pnp bipolar transistor. The emitter terminal of the second transistor Q3 is also coupled via a resistor R6 to a contact 14 of a momentary switch S1. Another contact 13 of the momentary switch S1 is coupled to the collector terminal of the transistor Q1 via a capacitor C1 and resistor R4 in parallel.

The contact 14 of the momentary switch S1 is also coupled to the base terminal of the second transistor Q3 and to the collector terminal of a third transistor Q2. The third transistor Q2 is an npn bipolar transistor. The base of the third transistor Q2 is coupled to the collector of the second transistor Q3 and the emitter of the third transistor Q2 is coupled to a ground potential 12 via a resistor R2. The collector of the second transistor Q3 is also coupled the ground potential 12 via resistor R3.

In parallel with the components described above is a capacitor C2 which is coupled between the collector of the first transistor Q1 and the ground potential 12. The capacitor C2 is also in parallel with the load R5.

The positive terminal of the battery 11 is coupled to the emitter terminal of the first transistor Q1 and the resistor R8 and the negative terminal of the battery 11 is coupled to the ground potential 12. However, alternatively, the negative terminal of the battery 11 may be coupled to a floating potential

In use, the switch circuit 10 operates as follows. Initially, with the momentary switch S1 in the position shown in Figure 1, the switch circuit 10 is in the off state and the transistors Q1, Q2 and Q3 are turned off. Hence, there is no closed circuit path and the switch circuit 10 acts to prevent a power being supplied from the battery 11 to the load R5.

When the switch circuit 10 is in the off state, the only power consumption is a reverse leakage power consumption through the transistors Q1, Q2, Q3 which is virtually negligible compared with the self discharging current of the battery 11.

Accordingly, the initial potential at the points 1, 2, 3, 4, 5, 6, 7, 8 in the circuit 10 and the status of the transistors are as follows:

The potential at point 3 = E (the potential of the battery 11);

The potential at point 1 = 0, as the transistor Q1 is switched off;

The potential across the base-emitter junction of the

first transistor $Q1 = 0$;

The potential at point 2 = the potential at point 3 = E ;

The current through $R1 = 0$;

The potential at point 7 = the potential at point
2 = E ;

The voltage across the base-emitter junction of the
second transistor $Q3 = 0$, as the second transistor $Q3$ is
switched off;

The potential at point 4 = the potential at point
7 = E ; Current through $R3 = 0$;

The potential at point 5 = 0 ;

The voltage across the base emitter junction of the
third transistor $Q2 = 0$;

The current through the resistor $R2 = 0$;

The potential at point 6 = 0 ;

The potential across the capacitor $C2 = 0$;

The potential across the capacity $C1 = 0$; and

The potential at point 8 = the potential at point
1 = 0 .

When the momentary switch $S1$ is pressed to complete the
contacts 13, 14 as shown in Figure 2 an initial closed circuit
(path A) is formed. This causes the base-emitter junctions of
the first and second transistors $Q1$, $Q3$ to be forward biased
thereby turning on transistors $Q1$, $Q3$. This generates an
initial current, contributing to the base current for the
first and second transistors $Q1$, $Q3$, which surges across the
resistor $R1$ through path A and rapidly drops to zero due to

the presence of the capacitor C1. This surge in base current drives the first and second transistors Q1, Q3 into saturation mode.

Simultaneously, the initial surge current passes through to resistor R3 (path B). As the voltage across R3 is raised rapidly due to the surge current, the base-emitter junction of the third transistor Q2 is forward biased thereby turning on the third transistor Q2. Similarly, the third transistor Q2 is also driven into saturation mode.

The third transistor Q2 takes its base current from the second transistor Q3 and at the same time, the third transistor supplies the base current to the second transistor Q3. Therefore, the voltage across the base-emitter junction of the second transistor Q3 is maintained forward biased with the third transistor Q2 in saturated mode as illustrated by path C while the voltage across the base-emitter junction of the third transistor Q2 is kept forward biased by the second transistor Q3 operating in saturated mode as shown by path B. In this way, without external current supply, the combination of the second and third transistors, Q3, Q2 will keep each other conducting as long as the battery 11 is coupled to the emitter of the second transistor Q3, that is the battery 11 is coupled to point 7 in the switch circuit 10. Therefore, the second and third transistors Q3, Q2 form a thyristor device which is triggered by the surge current generated in the switch circuit 10 when the momentary switch S1 is actuated.

Therefore, even when path A is open circuit due to the capacitor C1 being fully charged, the closed circuit path B and path C maintain the forward biasing of the base-emitter junctions of the second and third transistors Q3, Q2. In a similar manner, the base-emitter junction of the first transistor Q1 is also maintained in a forward biased mode with its base current driven into saturation mode.

Therefore, in this state the switch circuit 10 is turned on and power is supplied through the transistor Q1 to the load R5.

It should be noted that when momentary switch S1 is actuated to complete the contacts 13, 14 the capacitor C1 is charged up through path A. When capacitor C1 is fully charged, this prevents further current passing through the capacitor C1 and therefore, path A changes to open circuit. Therefore, it does not matter for how long the momentary switch S1 is actuated, as C1 will cause path A to go open circuit when it is fully charged. When the momentary switch S1 is released, the capacitor C1 will start to discharge through the resistor R4 to a zero charge state.

When the momentary switch S1 is actuated again to complete the contacts 13, 14 (see Figure 3) a closed circuit path D is formed in the switch circuit 10 as the capacitor C2 discharges. Therefore, the point 4 is momentary short circuited to point 8 during actuation of the switch S1.

However, when the capacitor C1 is fully charged, the capacitor C1 effectively make path D open circuit.

When the momentary switch S1 is pressed therefore, point 4 becomes the same potential as point 8 which is $E-0.2$ volts. However, the voltage at point 2 during the on state of the circuit 10 is $E-0.7$ volts. Therefore, when point 4 goes to $E-0.2$ volts, the base-emitter junctions of the first transistor Q1 and the second transistor Q3 are no longer forward biased and the first and second transistors Q1, Q3 are switched off. With the second transistor Q3 in its off mode, the base of the second transistor Q3 is also switched off which switches off the third transistor Q2. Therefore, the switch circuit 10 is switched off and as the first transistor Q1 is switched off, no power is supplied from the battery 11 to the load R5 and the remaining charge in the capacitor C2 discharges through the load R5.

After the capacitors C1 and C2 discharge completely, the switch circuit 10 reverse to the initial off state in which no power is supplied to the load R5 from the battery 11 and the only power consumed by the circuit 10 is the reverse leakage current through the first, second and third transistors Q1, Q3, Q2 which is virtually negligible.

A second example of a switch circuit 15 is shown in Figure 4. The switch circuit 15 is identical to the switch circuit 10, except that the circuit includes a signal input contact 16 at

point 5 of the circuit. The signal input contact 16 is connected to electronic equipment 17, which is the equivalent of the load R5 shown in Figures 1 to 3. The signal input contact 16 permits the electronic equipment 17 to turn itself off automatically, for example, after a predetermined period of time. The electronic equipment 17 turns the switch circuit 15 to the off state by applying a ground potential to the signal input contact 16 which switches off the third transistor Q2 which in turn switches off the second transistor Q3. This causes the switch circuit 15 to become open circuit which switches off the first transistor Q1 to cut off power supply from the battery 11 to the load 17.

Figure 5 shows a third example of a switch circuit 20 which is similar to the switch circuit 15 except a signal input contact 21 is connected at point 4. The signal input contact 21 when coupled to the electronic equipment 17 permits the electronic equipment 17 to switch off the switch circuit 20 by applying a high voltage state signal to contact 21. This causes the base emitter junction of the first and second transistors Q1, Q3 to be reversed biased which switches the first and second transistors Q1, Q3 off. With the first and second transistors Q1, Q3 switched off, the third transistor Q2 is also switched off as the potential at point 5 drops to zero and the switch circuit 20 is switched into the off state.

In Figures 4 and 5 it is important that the electrical connection from the electronic equipment 17 to the signal

input contact 16, 21 is maintained at a high impedance at all times except when a switch off signal is delivered to the signal input contact 16, 21.

Figure 6 shows a fourth example of a switch circuit 25. The switch circuit 25 is provided with a first switch signal input contact 16 connected to point 5 and a second switch signal input contact 21 connected to point 4. The switch circuit 25 controls the supply of power from the battery 11 to electronic equipment 26. The switch input contacts 16, 21 are coupled to a remote electronic system 27 which has its own power switch incorporated therein. The power switch incorporated within the remote electronic system 27 may be a switch circuit similar to any of the switch circuits 10, 15, 20, or may also be a switch circuit 25, controlled remotely by a further remote electronic system.

The switch circuit 25 permits remote power control from the other remote electronic system 27 and may be used for example, with a multi-unit system. The remote system 27 can switch the switch circuit 25 to the on state by applying a ground potential (or a sufficiently low level voltage) to the signal input contact 21 to forward bias transistor Q3.

Alternatively, the remote system 27 can switch the switch circuit 25 to the off state by applying a ground potential signal to signal input contact 16.

In all the switch circuits 15, 20, 25 a momentary switch S1 is

still provided which permits a user to manually switch circuits 15, 20, 25 between the off and on states.

As an alternative to the remote system being connected to separate input contacts 16, 21 it is possible that the remote system 27 could be connected by a single line to either the switch circuit 15 or the switch circuit 20. In the case of the switch circuit 15, the remote system 27 would switch on the circuit 15 by supplying a sufficiently high voltage level to the signal input contact 16 and switch off the circuit 15 by applying a ground potential to the signal input contact 16.

Where the remote system 27 is connected to signal input contact 21 in circuit 20, the remote system 27 would switch on the circuit 20 by applying a ground potential to the signal input contact 21 and switch off the circuit 20 by applying a sufficiently high voltage level to the signal input contact 21 to reverse bias the first and second transistors Q1, Q3.

Although the switches 10, 15, 20, 25 are shown controlling the supply of power from a battery 11 to load R5 or electronic equipment 17, 26, the circuits could also be used to control the supply of power from a rectified AC supply and from an AC main supply to electronic equipment having a heavy power consumption.

Figure 7 shows an example of the switch circuit 10 being used to control a rectified AC power supply from a transformer K2

and a full wave rectifier 29 to a load 28. However, switch circuit 10 could be replaced by any of switch circuits 15, 20, 25.

Figure 8 shows the switch circuit 10 being used to control power supply from an AC mains supply to a heavy load 30 through a transformer K2, a relay R, a diode D4 and a battery 32.

Figure 9 is a circuit diagram showing a fifth example of a switch circuit 40. The switch circuit 40 is identical to the switch circuit 10 except that the bipolar transistors Q1, Q2, Q3 are replaced by enhancement type MOSFETs M1, M2, M3 respectively. The transistors M1, M3 are P channel enhancement type MOSFETs and the transistor M2 is a N channel enhancement type MOSFET. The principle of operation of the switch circuit 40 is identical to the switch circuit 10.

Claims

1. A switch circuit for controlling the supply of electrical power from an electrical power source to a load, the switch circuit comprising a first transistor, the emitter of the first transistor adapted to be coupled to the power supply and the collector adapted to be coupled to the load; an electronic switching device comprising an input, an output adapted to be coupled to the other side of the load and the power source, and an activating input; a first resistance device coupled between the base of the first transistor and the input of the electronic switching device; a momentary switch having first and second terminals, the activating input of the electronic switching device coupled to the first terminal of the momentary switch; a pulse generation device coupled between the collector of the first transistor and the second terminal of the momentary switch; and a charge storing device coupled between the collector of the first transistor and the output of the electronic switching device.
2. A switch circuit according to claim 1, wherein the electronic switching device comprises a thyristor device.
3. A switch circuit according to claim 2, wherein the thyristor device comprises second and third transistors.
4. A switch circuit according to claim 3, wherein the base of the second transistor is coupled to the collector of the

third transistor, and the base of the third transistor is coupled to the collector of the second transistor.

5. A switch circuit according to claim 4, wherein the input of the electronic switching device is coupled to the emitter of the third transistor, the output is coupled to the emitter of the second transistor, and the activating input is coupled to the base of the third transistor and the collector of the second transistor.

6. A switch circuit according to any of the preceding claims, wherein the first transistor is a bipolar transistor.

7. A switch circuit according to any of claims 1 to 5, wherein the first transistor is a MOSFET.

8. A switch circuit according to claim 7, wherein the MOSFET is an enhancement type MOSFET.

9. A switch circuit according to claim 6 when dependent on any of claims 3 to 5, wherein the second and third transistors are bipolar transistors.

10. A switch circuit according to claim 7 or claim 8 when dependent on any of claims 3 to 5, wherein the second and third transistors are MOSFETs.

11. A switch circuit according to any of the preceding

claims, wherein the pulse generation device comprises a capacitance device.

12. A switch circuit according to claim 11, wherein the pulse generation device further comprises a third resistance device in parallel with the capacitance device.

13. A switch circuit according to any of the preceding claims, further comprising a first signal input contact coupled to the activating input of the electronic switching device.

14. A switch circuit according to any of claims 3 to 5, or any of claims 6 to 13 when dependent on any of claims 3 to 5, further comprising a second signal input contact coupled to the collector of the third transistor and the base of the second transistor.

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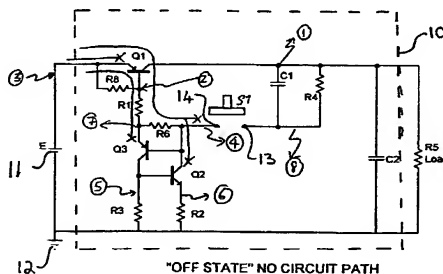
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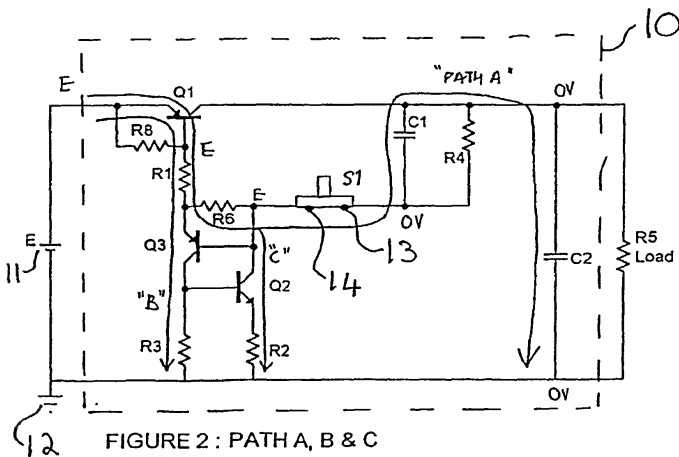
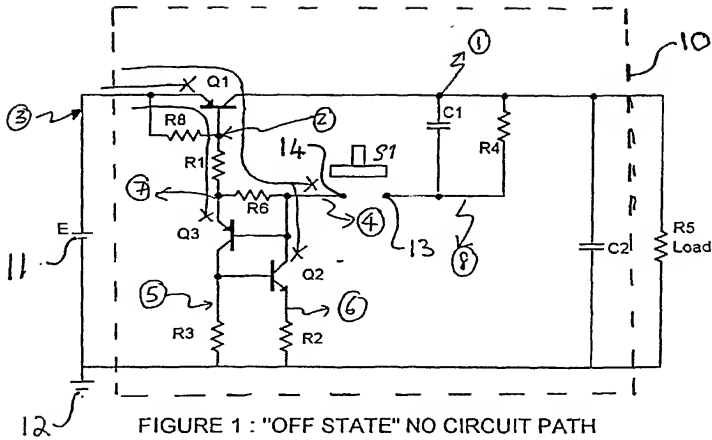
(54) Title: A SWITCH CIRCUIT



(57) Abstract: A switch circuit (10) controls the supply of electrical power from an electrical power source (11) to a load (R5). The switch circuit (10) includes a first transistor (Q1), the emitter of the first transistor (Q1) is adapted to be coupled to the power supply (11) and the collector is adapted to be coupled to the load (R5). An electronic switching device (Q2, Q3) includes an input, an output adapted to be coupled to the other side of the load (R5) and the power source (11), and an activating input. A first resistance device (R1) is coupled between the base of the first transistor (Q1) and the input of the electronic switching device (Q2, Q3). A momentary switch (S1) has first and second terminals (13, 14) and the activating input of the electronic switching device (Q2, Q3) is coupled to the first terminal (14) of the momentary switch. A pulse generation device (C1, R4) is coupled between the collector of the first transistor (Q1) and the second terminal (13) of the momentary switch (S1). A charge storing device (C2) is coupled between the collector of the first transistor (Q1) and the output of the electronic switching device (Q2, Q3).

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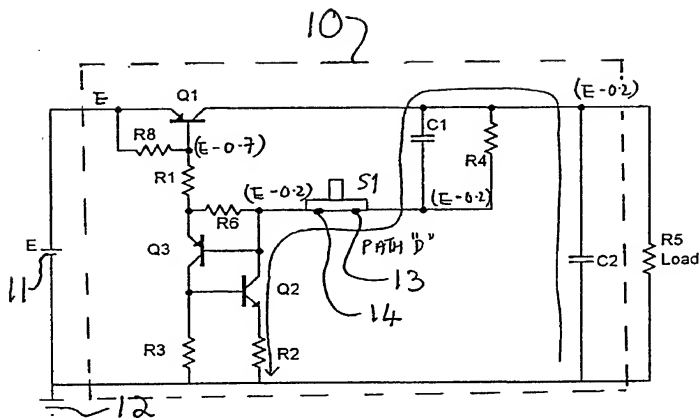


FIGURE 3 : PATH D

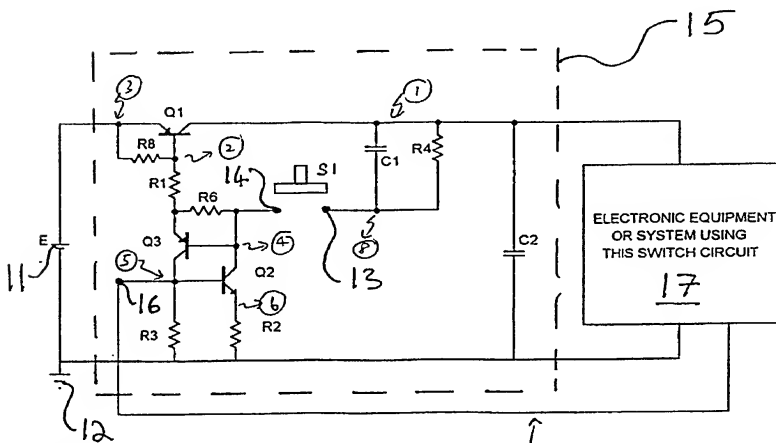


FIGURE 4 AUTOMATIC POWER DOWN WITH ELECTRICAL CONNECTION AT POINT (5)

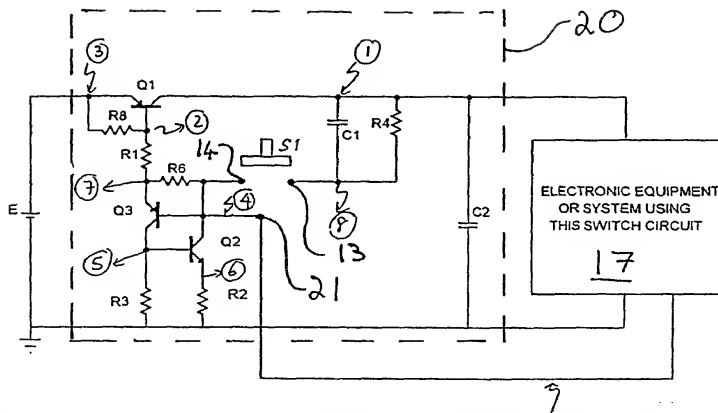


FIGURE 5 : AUTOMATIC POWER DOWN WITH ELECTRICAL CONNECTION AT POINT (4)

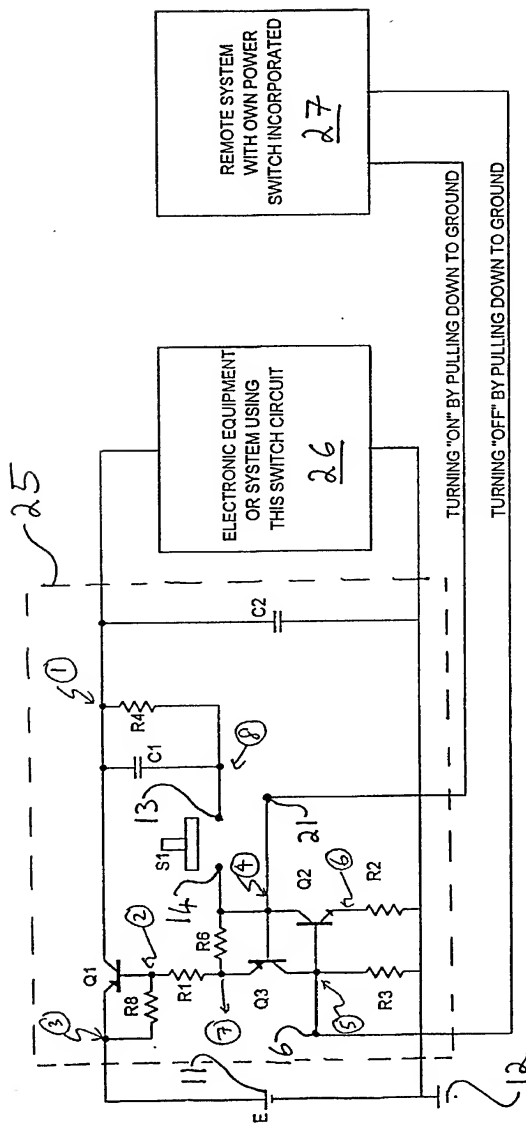


FIGURE 6: REMOTE CONTROL FROM ANOTHER SYSTEM, EXAMPLE ***

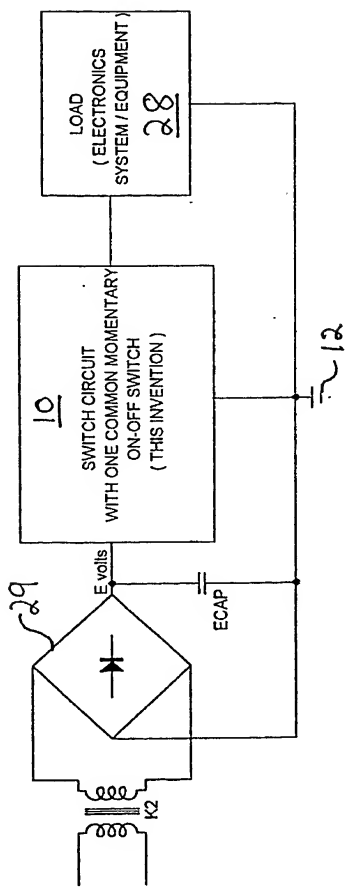


FIGURE 7

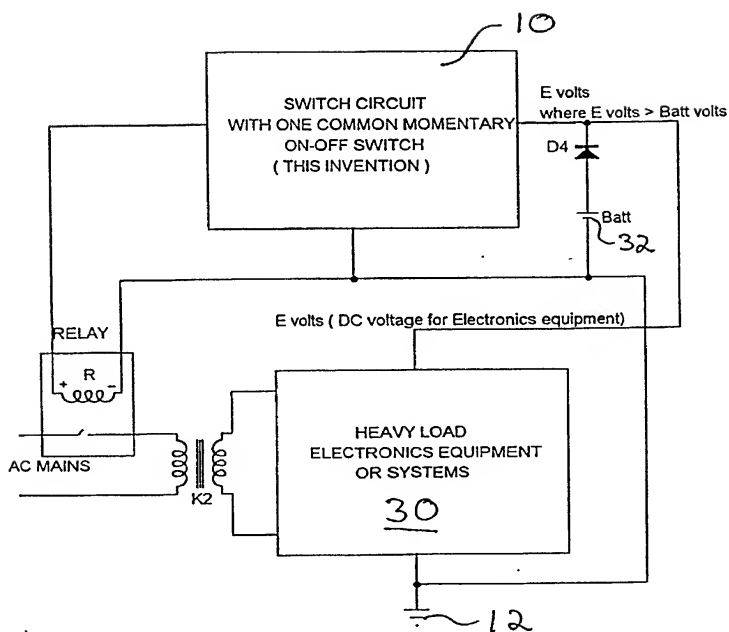


FIGURE 8

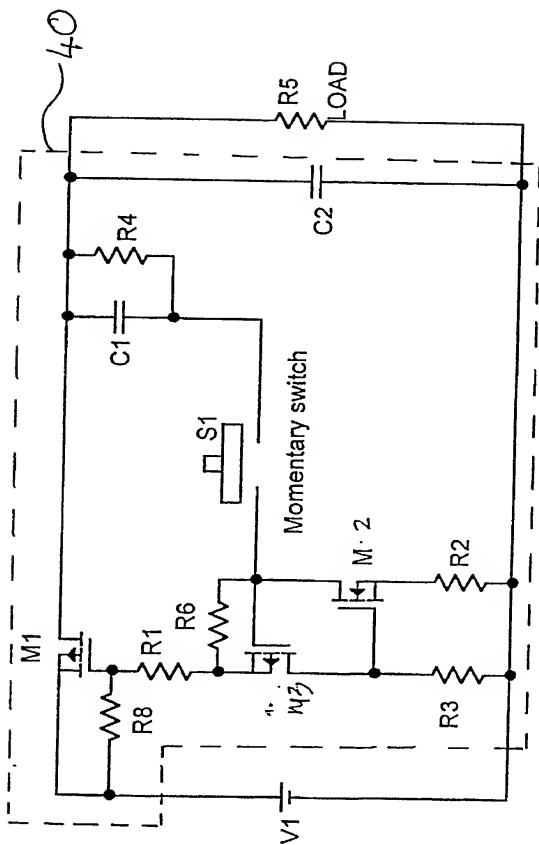


Figure 9

	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION		OFGS FILE NO P/2778-25																																																
<p>As the named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled</p> <p>A SWITCH CIRCUIT</p> <p>the specification of which is attached hereto, unless the following box is checked</p> <p><input checked="" type="checkbox"/> was filed on <u>13 August 1999</u> as United States patent Application Number or PCT International patent application number <u>PCT/SG99/00084</u> and was amended on _____ (if any)</p> <p>I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above</p> <p>I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.</p> <p>I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed</p> <p>Prior Foreign or Provisional Application(s)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">COUNTRY</th> <th style="width: 35%;">APPLICATION NUMBER</th> <th style="width: 20%;">DATE OF FILING (day, month, year)</th> <th style="width: 20%;">PRIORITY CLAIMED UNDER 35 U.S.C. 119</th> </tr> </thead> <tbody> <tr> <td> </td> <td> </td> <td> </td> <td>YES <input type="checkbox"/> NO <input type="checkbox"/></td> </tr> <tr> <td> </td> <td> </td> <td> </td> <td>YES <input type="checkbox"/> NO <input type="checkbox"/></td> </tr> </tbody> </table> <p>I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 40%;">UNITED STATES APPLICATION NUMBER</th> <th style="width: 30%;">DATE OF FILING (day, month, year)</th> <th style="width: 30%;">STATUS (patented, pending, abandoned)</th> </tr> </thead> <tbody> <tr> <td> </td> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> </tbody> </table> <p>I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Max Moskowitz - Reg. No. 30,576; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944; Louis C. Dujmeh - Reg. No. 30,625; and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.</p> <p>SEND CORRESPONDENCE TO: OSTROLENK, FABER, GERB & SOFFEN, LLP DIRECT TELEPHONE CALLS TO 1180 AVENUE OF THE AMERICAS (212) 382-0700 NEW YORK, NEW YORK 10036-8403 CUSTOMER NO. 2352</p> <p>I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">FULL NAME OF SOLE OR FIRST INVENTOR Jun MAKINO</td> <td style="width: 30%;">INVENTOR'S SIGNATURE </td> <td style="width: 30%;">DATE 18 APR 2002</td> </tr> <tr> <td>RESIDENCE (City and either State or Foreign Country) Singapore 669555, Singapore</td> <td colspan="2">COUNTRY OF CITIZENSHIP Japan</td> </tr> <tr> <td colspan="3">POST OFFICE ADDRESS 19B, Hillview Avenue, #12-05 Hillview Park, Singapore 669555, Singapore</td> </tr> <tr> <td>FULL NAME OF SECOND JOINT INVENTOR (IF ANY)</td> <td>INVENTOR'S SIGNATURE</td> <td>DATE</td> </tr> <tr> <td>RESIDENCE (City and either State or Foreign Country)</td> <td colspan="2">COUNTRY OF CITIZENSHIP</td> </tr> <tr> <td colspan="3">POST OFFICE ADDRESS</td> </tr> <tr> <td>FULL NAME OF THIRD JOINT INVENTOR (IF ANY)</td> <td>INVENTOR'S SIGNATURE</td> <td>DATE</td> </tr> <tr> <td>RESIDENCE (City and either State or Foreign Country)</td> <td colspan="2">COUNTRY OF CITIZENSHIP</td> </tr> <tr> <td colspan="3">POST OFFICE ADDRESS</td> </tr> </table>			COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119				YES <input type="checkbox"/> NO <input type="checkbox"/>				YES <input type="checkbox"/> NO <input type="checkbox"/>	UNITED STATES APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)							FULL NAME OF SOLE OR FIRST INVENTOR Jun MAKINO	INVENTOR'S SIGNATURE 	DATE 18 APR 2002	RESIDENCE (City and either State or Foreign Country) Singapore 669555, Singapore	COUNTRY OF CITIZENSHIP Japan		POST OFFICE ADDRESS 19B, Hillview Avenue, #12-05 Hillview Park, Singapore 669555, Singapore			FULL NAME OF SECOND JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE	RESIDENCE (City and either State or Foreign Country)	COUNTRY OF CITIZENSHIP		POST OFFICE ADDRESS			FULL NAME OF THIRD JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE	RESIDENCE (City and either State or Foreign Country)	COUNTRY OF CITIZENSHIP		POST OFFICE ADDRESS		
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